

CLAIMS

1. A data scrambler, comprising:
a scrambler device configured to scramble a parallel array of input bits into an array of scrambled output bits all during a same current clock period.
2. A data scrambler according to claim 1 including a new seed register for storing the scrambled output bits from a previous clock period and supplying the scrambled output bits to the scrambler device for applying to the parallel array of input bits during the current clock period.
3. A data scrambler according to claim 1 wherein the scrambler device generates an array of polynomial values for applying to the parallel array of input bits by feeding back an array of scrambled output bits generated during a previous clock period.
4. A data scrambler according to claim 3 including a seed register for storing the array of scrambled output bits.
5. A data scrambler according to claim 3 wherein the scrambler device selects the scrambled output bits for applying to each one of the input bits according to a polynomial value, a bit length for the parallel array of input bits, and a position of the input bits in the parallel array.

5 6. A data scrambler according to claim 1 wherein a $1 + X(39) + X(58)$ scramble polynomial is applied to each bit of the parallel array of input bits according to the following:
Dout[0:38] = NS[38:0] ^ NS[57:19] ^ Din[0:38];
Dout[39:57] = NS[18:0] ^ NS[38:20] ^ NS[57:39] ^ Din[0:18] ^ Din[39:57]; and
Dout[58:N] = NS[19:14] ^ NS[57:52] ^ Din[0:5] ^ Din[19:24] ^ Din[58:63]; where, Dout are
10 the scrambled output bits generated during the current clock period, Din are the input bits,
NS[57:0] = Dout'[M : N], M = N - 58, N = 64, and Dout' are the scrambled output bits
generated during a previous clock period.

15 7. A data scrambler according to claim 2 including an input data register
configured to output the parallel array of input bits to the scrambler device and an output data
register for receiving the array of scrambled output bits from the scrambler device.

20 8. A data scrambler according to claim 1 wherein an output of the scrambler
device is coupled to both the output data register and the new seed register and an output of
the new seed register is coupled to the scramble device.

25 9. A data scrambler according to claim 1 including an ingress buffer manager
that uses the scrambler device to scramble the array of input bits from network packets
transferred over a switch fabric.

 10. A data scrambler according to claim 1 including an egress network processor
that uses the scrambler device to scramble the array of input bits from network packets sent
over a network.

11. A method for scrambling data, comprising:

receiving a parallel array of input bits;

storing an array of previously scrambled output bits from a previous clock period; and

applying the array of previously scrambled output bits to the parallel array of input

10 bits during a same current clock period to generate a current array of scrambled output bits.

12. A method according to claim 11 including storing the previous scrambled
output bits from the previous clock period as new seed values for applying scramble
polynomials to each of the parallel array of input bits during the same current clock period.

13. A method according to claim 12 including selecting the new seeds values
according to scramble polynomial values, a bit length of the parallel array of input bits, and a
position of the individual bits in the parallel array of input bits.

14. A method according to claim 11 including using the stored array of previously
scrambled output bits to apply a $1 + X(39) + X(58)$ scramble polynomial to each one of the
parallel array of input bits during the same current clock period.

15. A method according to claim 11 including:

receiving a parallel array of scrambled input bits;

storing an array of previously de-scrambled output bits de-scrambled during a
previous clock period; and

5 applying the array of previously de-scrambled output bits to the parallel array of
scrambled input bits during a same current clock period to generate a current array of de-
scrambled output bits.

16. A method according to claim 15 including storing the current array of de-
10 scrambled output bits as new seed values for applying to a next parallel array of scrambled
input bits during a next clock period.

17. A method according to claim 11 including:
scrambling the parallel array of input bits for network packets in a network router;
15 transferring the network packets over a switch fabric in the network router; and
de-scrambling the scrambled parallel array of input bits received over the switch
fabric.

18. A method according to claim 11 including:
20 de-scrambling a parallel array of scrambled packet bits received over a network; and
scrambling parallel arrays of de-scrambled packet bits during the same clock period
before sending the packet bits over the network.

19. A network processing device, comprising:
25 an ingress circuit configured to process packets received over a network;
an egress circuit configured to process packets for sending over the network;
a switch fabric for transferring packets between the ingress circuit and the egress
circuit; and

5 a scrambler circuit configured to scramble a parallel array of packet bits into an array of scrambled output bits during a same current clock period.

20. A network processing device according to claim 19 including a new seed register for storing an array of scrambled output bits from a previous clock period and
10 supplying the array of scrambled output bits to the scrambler circuit for applying to the parallel array of packet bits during the current clock period.

21. A network processing device according to claim 20 including a first scrambler circuit and new seed register located in the ingress circuit for scrambling the array of packet
15 bits before being transferred over the switch fabric and a second scrambler circuit and new seed register located in the egress circuit for scrambling the array of packet bits before being transferred over the network.

22. A network processing device according to claim 20 including a de-scrambler
20 circuit configured to de-scramble the array of scrambled packet bits into an array of de-scrambled packet bits during a same current clock period.

23. A network processing device according to claim 22 including a de-scrambler new seed register for storing an array of de-scrambled packet bits from a previous clock
25 period and supplying the array of de-scrambled output bits to the de-scrambler circuit for applying to the scrambled packet bits during the current clock period.

